REMARKS

Claims 9-13, 22-26, 32, 37, 38, 40-46 and 48-57 are all the claims pending in the application.

Support for the amendments to the claims may be found in the specification as originally filed, for example:

Claims 9, 11 & 12	The claims as originally filed and at lines 24 to 27 on page 24 and at lines 5 to 9 on page 31;.
Claim 13	Claim 13 as originally filed;
Claim 23	Claim 23 as originally filed and at line 31 on page 39 to line 10 on page 40;
Claim 24	Claim 24 as originally filed and at line 12 on page 48 to line 24 on page 49;
Claim 25	At line 13 on page 34 to line 29 on page 3;
Claim 32	At lines 4 to 11 on page 55;
Claim 37	Fig. 36;
Claims 40 & 41	Figs. 44, 45 and 49;
Claim 42	Figs. 46 and 50;
Claim 44	Claim 44 as originally filed;
New Claims 48, 49 & 51	At lines 18 to 22 on page 25 in the specification;
New Claim 50	Claim 13 as originally filed;
New Claims 52 & 54	At lines 16 to 24 on page 49;
New Claim 53	Fig. 16 and at lines 13 to 16 on page 33;
New Claim 55	At lines 1 to 5 on page 39;
New Claim 56	At lines 6 to 19 on page 39; and
Claim 57	Fig. 23.

I. The Rejection under 35 U.S.C. §102(e) Based on Yasue

Claims 22-26, 32, 37, 38, 40-42 and 44-46 are rejected under 35 U.S.C. §102(e) as allegedly being anticipated by US Patent 6,251,502 (Yasue).

Applicants respectfully submit that the present invention is not anticipated by or obvious over the disclosures of Yasue and request that the Examiner reconsider and withdraw this rejection in view of the following remarks.

A. Claim 22 and newly added Claim 52

Conventional electroless plated film is formed by an electroless plating solution containing EDTA as a complexing agent. However, a compressive stress (an expanding force) is generated in such an electroless plated film. That is, negative stress (less than 0 kg/mm^2) is generated.

Therefore, an electroless plated film formed on a resin insulating layer comprising a roughened surface tends to expand or stretch owing to the compressive stress, and thus peels from the resin surface.

On the other hand, if the stress of the electroless plated film exceeds +10 kg/mm^2, the stress is focused on the inside of the electroless plated film. Adhesion of the electroless plated film to the resin insulating layer comprising a roughened surface is deteriorated by this stress. This causes problems such as peeling and fracture of the electroless plated film.

Furthermore, when a plane layer such as a power layer is formed from a conventional electroless plated film obtained by a plating solution containing EDTA as a complexing agent, the plane layer must be formed into a mesh. An electroless plated film in a mesh form can buffer stress since transmission of the stress is prevented in the area where no electroless plated film is present, and thus peeling of electroless plated film is suppressed.

However, it has been discovered that, in the case where a plane layer is formed into a mesh, a conductor circuit may be undulated when it is formed on a resin insulating layer which is formed on the mesh plane layer, or deterioration of electric properties such as a lack of or insufficient impedance alignment may occur.

To the contrary, an electroless plated film according to the present invention has a stress of 0 to +10 kg/mm^2 (Claim 22). As its tensile strength is appropriate, the electroless plated film adheres to the resin insulating layer without peeling. Even if it is not in a mesh form, the electroless plated film does not peel from the resin insulating layer.

Among electroless plated films comprising a stress of 0 to +10 kg/mm^2, an electroless plated film formed by a plating solution comprising tartaric acid or a salt thereof adheres intimately to the resin insulating substrate and hardly peels off from the substrate since the amount of hydrogen uptake in the plated film is small and a tensile stress (a stress counter to a compressive stress) is generated in the plated film.

Yasue discloses a method of forming an electroless plated film on a roughened surface by an electroless plating solution containing EDTA (see Table 1). Yasue does not teach or suggest the stress of the electroless plated film. In fact, since EDTA is contained in the electroless plating solution, a compressive stress is generated in the plated film. As a result, a slight peeling (swelling) is observed in the board of Example 1 (col. 26, lines 33-35). Applicants submit that the stress generated is not within the range of 0 to +10 kg/mm^2, and the electroless plated film according to Yasue is not within the scope of Applicants' claimed invention.

Applicants respectfully submit that the present invention is not anticipated by and not obvious over Yasue.

B. Claim 23 and newly added Claim 53

The present invention discloses an electroless plated film complementary to a roughened surface of a resin insulating substrate board comprising convex areas and concave areas, the electroless plated film in convex areas of the roughened surface being relatively greater in thickness than the electroless plated film in concave areas of the roughened surface (Claim 23). As shown in attached Fig. 1, the thickness A is greater than the thickness B.

The conductor circuit according to the present invention is built by semi-additive process. It is required to etch a part of an electroless plated film built on above-mentioned roughened surface (page 40, lines 3-10).

The film in concave areas of the roughened surface is less exposed to etchant than the film in the convex areas. Therefore, the conductor in concave areas of the roughened surface tends to be left unetched. This phenomenon may occur especially when the electroless plated film in concave areas of the roughened surface is substantially the same or greater in thickness than the film in convex areas of the roughened surface. Such unetched conductor residue causes a short circuit, or generates a crack of a resin layer.

To prevent the problems caused by unetched conductor residue, it is required to prolong the etching time or increase the concentration of the etchant so that the electroless plated film in concave areas is stripped off completely. However, excess etching treatment causes problems such as thinning down of the conductor circuit and undercut of the conductor circuit.

To the contrary, an electroless plated film comprising the constitution according to the present invention allows the electroless plated film in concave areas to be stripped off completely as long as the etching condition is capable of removing the electroless plated film in convex areas. Above-mentioned problems

are not caused, and electric connection and reliability of conductor circuit are improved.

Fig. 5C in Yasue shows that the thickness (B) of electroless plated film in concave areas of the roughened surface is greater than the thickness (A) of the electroless plated film in convex areas of the roughened surface (see attached Fig. 2).

Therefore, the electroless plated film according to Yasue is different in constitution from the electroless plated film according to the present invention. If such an electroless plated film is etched, the electroless plated film in concave areas may be left unetched.

The conductor circuit in Yasue is formed by full-additive method. That is, conductor circuit is built by electroless plating treated on the part where no plating resist is present. In this method, it is not required to remove the electroless plated film once formed. Therefore, no conductor residue on the roughened surface is left unetched.

Accordingly, Yasue does not provide any motivation to one of ordinary skill in the art to obtain the electroless plated film of the present invention. Applicants respectfully submit that the electroless plated film of the present invention is not anticipated by and not obvious over Yasue.

C. Claim 24 and newly added Claims 54 and 55

According to the present invention, via holes are formed by carrying out electroless plating on the whole surface of interlayer resin insulating layer having openings for via holes. The electroless plated film formed on the bottoms of the via holes have a thickness equal to 50 to 100% of the thickness of the electroless plated film on the interlayer resin insulating layer.

If the electroless plated film formed on the bottoms of the via holes has a thickness less than 50% of the thickness of the electroless plated film on the

interlayer resin insulating layer, the film on the bottoms of the via holes is not necessarily formed in compliance with the roughened surface, thus deteriorates the adhesion of the film, electric connection and reliability.

Further, if a plated film (in the present invention, an electroplated film) is formed on the electroless plated film, the electroless plated film functions as cathode. However, if the electroless plated film formed on the bottoms of the via holes has a thickness less than 50% of the thickness of the electroless plated film on the interlayer resin insulating layer, it does not function as cathode, and the formation of an electroplated film is suppressed.

On the other hand, if the electroless plated film formed on the bottoms of the via holes has a thickness greater than 100% of the thickness of the electroless plated film on the interlayer resin insulating layer, compliance of the electroless plated film formed within via holes with the roughened surface is canceled. Thus, adhesion effect of anchors on the roughened surface of the electroless plated film is diminished, resulting in the decrease of the reliability of the printed circuit board.

According to the present invention (Claim 54), the electroless plated film is formed by an electroless plating solution comprising tartaric acid or a salt thereof. It can buffer a stress in the film and therefore prevent the peeling of the electroless plated film especially in the vicinity of via holes.

Even when the openings for via holes are as fine as 80 μm or less in diameter, via holes capable of insuring appropriate connection of metal are formed as long as the thickness of the electroless plated film on the hole bottoms is within the above-mentioned range. Therefore, electric connection and reliability are insured.

Yasue discloses a method to form an electroless plated film on a roughened surface. However, Yasue does not mention or suggest the appropriate range of film thickness. Further, the electroless plated film is formed on via holes with a diameter of about 100 μm. The electroless plating solution comprises EDTA.

Accordingly, the electroless plated film of the present invention is different in constitution from that of Yasue and the effect of the present invention is not described in Yasue. Yasue does not provide any motivation to one of ordinary skill in the art to obtain the electroless plated film of the present invention.

Applicants respectfully submit that the present invention is not anticipated by and not obvious over Yasue.

D. Claims 25, 26 and newly added Claim 56

According to the present invention, the electroless plated film is a copper film and comprises at least one metal species selected from the group consisting of nickel, iron and cobalt (Claim 25).

Addition of a salt of such a metal ion reduces the compressive stress of the electroless plated film so that the resulting film may have an improved adhesion to the resin insulating layer, and peeling of the plated film is prevented.

Further, addition of such a metal species increases the hardness of the plated film, and stress in the film can be buffered in the film itself. Therefore, problems attributed to the stress do not occur, and a conductor circuit comprising the electroless plated film formed as claimed has improved electric connection and reliability.

It is preferable that the content of at least one metal species selected from the group consisting of nickel, iron and cobalt is within the range of 0.1 to 0.5 weight % (Claim 26). If the content is less than 0.1 weight %, it is difficult to increase the hardness, and the stress in the film cannot be buffered. On the other hand, if the content is more than 0.5 weight %, the hardness of the film is so high that the roughened surface may be damaged or other problems may occur.

Yasue discloses a method to form an electroless plated film on a roughened surface. For example, the table in column 25 shows an electroless plating solution containing two metal complex. However, a major component of this plating solution

is nickel. The effect of the present invention as mentioned above cannot be attained by this method.

Further, Yasue does not indicate that the content of metal is within above-mentioned range. Yasue teaches that a desirable amount of nickel is about 1-5% (col.14, lines 55 to 58), however, it is different from the desirable content according to the present invention. The table in column 25 shows that the content of nickel (95.1 mM) is about sixteen times as many as that of copper (6.0 mM).

Yasue discloses full-additive method of electroless plating.

Accordingly, the electroless plated film of the present invention is different in constitution from that of Yasue, and Yasue does not provide any motivation to one of ordinary skill in the art to obtain the electroless plated film of the present invention. Applicants respectfully submit that the printed circuit board of the present invention is not anticipated by and not obvious over Yasue.

E. Claim 32 and New Claim 57

According to the present invention, the thickness of the conductor circuit on the core board is not greater by more than 10 μm than the thickness of the conductor layer on the interlayer resin insulating layer, and the thickness of the conductor circuit on the core board is substantially the same as the thickness of the conductor layer on the interlayer resin insulating layer (Claim 32). Under this condition, an impedance alignment can be easily attained and electrical properties are improved.

If the thickness of one of them differs largely from the other, a heat cycle-associated stress may develop. If the stress is not buffered, it becomes a cause of cracks in the interlayer resin insulating layer.

In Example 10 in Yasue, a copper foil 12 on substrate 1 has a thickness of 18 μm (col.23, line 40), and a photoresist at a thickness of 60 μm is applied to the surface of the resin insulating layer (col.25, lines 32 to 34). It indicates that the

thickness of the conductor layer on the resin insulating layer is about three times as many as the thickness of the conductor circuit on core board.

Accordingly, the multilayer printed circuit board of the present invention is different in constitution from that of Yasue. There is no motivation for one of ordinary skill in the art to attain the present invention from the disclosures of Yasue. Applicants respectfully submit that the present invention is not anticipated by and not obvious over Yasue.

F. Claims 37 and 38

In the multilayer printed circuit board of the present invention, via holes are formed immediately over plated-through holes in the core board in the manner of plugging the through holes in the plated-through holes and are interconnected with the plated-through holes (Claim 37).

In the multilayer printed circuit board of the prior art, a land is formed around a through hole and a via hole is connected with this land. It is impossible to connect the via hole with the through hole unless the land is teardrop or potbelly shaped (see US Patent 6, 342, 682). With this constitution, space for the land is a dead space and high density layout of plated-through holes cannot be attained.

To the contrary, in the multilayer printed circuit board according to the present invention, as the land configuration can be of small area (true-round for example) and the region immediately over the plated-through holes is allowed to function as an internal layer pad, the dead space is eliminated. As a result, the layout density of plated-through holes in the multilayer core board can be increased, and the number of layers can be minimized by equating the number of layers of the upper-layer multilayer circuit stratum to the number of layers of the lower--layer multilayer circuit stratum. Furthermore, since the via hole is disposed immediately over the plated-through hole, the wiring length can be reduced to increase the

signal transmission speed. A multilayer printed circuit board of high density and superior electric properties can be thus obtained.

Figs. 3A-3I in Yasue disclose a multilayer printed circuit board comprising a core board (1) having plated-through holes (13) and, as constructed on both sides thereof, conductor layers (5, 5', 6 and 6') and interlayer resin insulating layers (2 and 3) alternately with conductor layers being interconnected by via holes (Office Action). In Fig. 3I, it is shown that via holes 9 are disposed over the plated-through holes through the intermediary of interlayer resin insulating layers.

However, via holes are not disposed immediately over the plated-through holes. Via holes and plated-through holes are not interconnected directly, since insulating layers are disposed over the plated-through holes. Therefore, it is understood that via holes and plated-through holes are interconnected through conventional lands, and longer wiring length is required. With such a constitution, the effect of the present invention cannot be realized.

Accordingly, the multilayer printed circuit board of the present invention is different in constitution from that of Yasue. Applicants respectfully submit that the present invention is not anticipated by and not obvious over Yasue.

G. Claims 40 to 42 and 44 to 46

In the multilayer printed circuit board according to the present invention, in the similar manner described in (1-6), the plated-through hole, the lower-layer via hole and the upper-layer via hole are interconnected in alignment.

Therefore, the wiring length can be reduced and the signal transmission speed can be increased.

This constitution is different from that disclosed in Yasue. Applicants respectfully submit that the subject matter of claims 40-42 and 44-46 is not anticipated by and not obvious over Yasue.

For the above reasons, it is respectfully submitted that the subject matter of claims 22-26, 32, 37, 38, 40-42 and 44-46 is neither taught by nor made obvious from the disclosures of Yasue and it is requested that the rejection under 35 U.S.C. §102 be reconsidered and withdrawn.

II. The Rejection under 35 U.S.C. §103 Based on Yasue and Ono

Claim 43 is rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Yasue in view of US Patent 6,217,987 (Ono).

Applicants respectfully submit that the present invention is not obvious over the disclosures of Yasue and Ono and request that the Examiner reconsider and withdraw this rejection in view of the following remarks.

As discussed above, independent Claims 40 to 42 are not anticipated by or obvious over Yasue. Ono does not overcome the deficiencies in the primary reference Yasue discussed above.

For the above reasons, it is respectfully submitted that the subject matter of claim 43 is neither taught by nor made obvious from the disclosures of Yasue and Ono and it is requested that the rejection under 35 U.S.C. §103 be reconsidered and withdrawn.

III. The Rejection under 35 U.S.C. §103 Based on Miyabayashi and Shimamoto

Claims 9 to 13 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over US Patent 4,777,078 (Miyabayashi) in view of US Patent 5,780,143 (Shimamoto).

Applicants respectfully submit that the present invention is not obvious over the disclosures of Miyabayashi and Shimamoto and request that the Examiner reconsider and withdraw this rejection in view of the following remarks.

The present invention discloses a copper film comprising an electroplated layer and having properties that (a) its crystallinity is such that the X-ray diffraction half-width of the (331) plane of copper is less than 0.3 deg. and (b) the variation in thickness ((maximum thickness-minimum thickness) /average thickness) of the copper film as measured over the whole surface of the substrate is not greater than 0. 4.

If crystallinity of a film is such that the X-ray diffraction half-width of the (331) plane of copper is less than 0.3 deg., a highly uniform thickness of electrodeposition and an increased crystallinity of the film are insured, and the residual stress in the electroplated layer is low. Therefore, it is desirable that half width is less than 0.3 deg. in view of the crystallinity.

On the contrary, if the X-ray diffraction half-width is 0.3 deg. or more, the copper layer has poor crystallinity and large residual stress. Fine-line patterns comprising such copper plating layer tend to peel easily.

In X-ray diffraction analysis of metal such as copper, diffraction width tends to broaden at higher angle in the same sample. The X-ray diffraction half-width of copper film at a higher angle, the (331) plane for example, is higher than that at a lower angle, the (200) plane shown in Miyabayashi for example.

Attached Figs. 3 and 4 show the results of X-ray diffraction analysis of plated copper films according to the present invention. X-ray diffraction half-width is larger at a higher angle than at a lower angle. When the half-width of the X-ray diffraction intensities on the (200) plane of copper coating is 0.25 deg., thus, measurement at higher angle is accompanied by broader half-width exceeding 0.30 deg.

X-ray diffraction analysis at a low angle tends to detect much amount of noise. This is attributed to X-ray measurement itself (scattering of X-ray,

measurement angle and the like), sample to be measured (uneven surface condition, error of device) and the like.

To the contrary, measurement at a high angle, the (331) plane shown in the present invention for example, displays the change in crystallinity clearly and indicates less amount of noise since the measurements are made at a high angle. It is possible to measure the copper plated film with high accuracy and highly reproducible results.

Although the plated film according to the present invention is measured at a high angle, the half width is less than 0.3 deg. The results obtained by the measurement at the (331) plane are not affected by noise and vividly illustrates the crystallinity. Evaluation of properties of the plated film according to the present invention is not carried out by simply comparing the measurement results. Rather, properties have specific relation to measurement angle and half width of X-ray diffraction analysis.

Miyabayashi discloses the results of the X-ray diffraction analysis, however, the measurement is not carried out on the (331) plane.

Further, Miyabayashi shows that the half width of the X-ray diffraction intensities on the (200) plane of copper coating is 0.25 deg. (col. 6, lines 41 to 46). As mentioned above, measurement at a higher angle is accompanied by broader diffraction width. Thus, the half width of the X-ray diffraction intensities at the (331) plane of copper coating according to Miyabayashi should exceed 0.3 deg. Therefore, the copper coating according to Miyabayashi is different in constitution from the plated film according to the present invention.

The printed circuit board of the present invention further comprises the property (b) so that it keeps the flatness of the circuit and does not disturb the signal wires which are connected. Thus, it is capable of facilitating the impedance alignment.

On the contrary, if the variation in thickness ((maximum thickness-minimum thickness)/average thickness is over 0.4, the circuit may have undulation. Thus, impedance alignment cannot be facilitated with the connected signal wires. It also causes problems with electric properties.

Miyabayashi discloses a method of forming a copper coating formed by chemical plating (electroless plating). It mentions: If it is possible to form a mechanically excellent copper coating solely by the chemical or electroless plating process, the conventional need of an additional electroplating step and the electrical equipment therefore can be eliminated, and the economical advantage of the chemical plating can be enjoyed (col. 1, line 65 to col. 2, line 2). Thus, it is apparent that Miyabayashi has a negative view on electroplating step. Miyabayashi does not provide any motivation, but rather teaches away from the present invention.

In addition, the plating solution used in Miyabayashi contains EDTA as a complexing agent.

Additionally, plated copper film according to the present invention comprises an electroplated layer.

The claims of the present invention disclose a plated copper film which is different in constitution from Miyabayashi and is not anticipated by and not obvious over Miyabayashi.

Shimamoto is related to a circuit board comprising a through-hole filled with an electrically conducting substance. The electrically conducting substance is composed of a cured product of a curable electrically conducting substance. Shimamoto discloses electrically conducting patterns having an average thickness of 25 μm (fluctuation of about ±10%) (col. 18, lines 53 to 54).

However, Shimamoto mentions: According to the above-mentioned method (a) of forming the circuit board, however, plating must be effected more than two times to enhance reliability of the connection means, which is not necessarily

advantageous from the standpoint of cost. Besides, since the electroplating is effected for the whole surfaces of the board body, the thickness of the electrically conducting layers becomes irregular, and etching for forming the circuit patterns is effected unevenly. Therefore, this method is not suited for obtaining circuit boards having fine circuit patterns (col. 1, 20, lines 34 to 43). Accordingly, it is understood that Shimamoto has a negative view and teaches away from an electroplating method for forming circuit patterns.

Further, Shimamoto does not disclose results of X-ray diffraction analysis. Thus, Shimamoto does not teach or disclose that a plated film with property (a) according to the present invention has highly uniform thickness of electrodeposition.

Moreover, production of the circuit board according to Shimamoto requires a step of curing electrically conducting substance. This curing step is carried out at a high temperature (160°C in Examples 1 to 5). Under such a treatment, an oxidized film is formed on the surface and lowers degree of crystallinity. Therefore, it is clear that Shimamoto does not mention or suggest the copper film according to the present invention and the effect thereof.

For the above reasons, each of the cited references is quite different from the invention and does not render obvious Applicants' claimed invention. Moreover, even if the cited references are combined, it is respectfully submitted that it would not have been obvious to one of ordinary skill in the art to select the inventive printed circuit board which overcomes problems in the art.

For the above reasons, it is respectfully submitted that the subject matter of claim 9 to 13 is neither taught by nor made obvious from the disclosures of Miyabayashi and Shimamoto and it is requested that the rejection under 35 U.S.C. §103 be reconsidered and withdrawn.

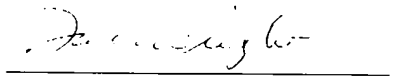
IV. Conclusion

In view of the above, Applicants respectfully submit that their claimed invention is allowable and ask that the rejections under 35 U.S.C. §102 and §103 be reconsidered and withdrawn. Applicants respectfully submit that this case is in condition for allowance and allowance is respectfully solicited.

If any points remain at issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the local exchange number listed below.

Applicants hereby petition for any extension of time which may be required to maintain the pendency of this case. The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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APPENDIX
VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The specification is changed as follows:

The last paragraph on page 80 is amended as follows:

The results of this evaluation are presented in [Table 1] Figure 4. The smaller the value is, the higher is the uniformity of electrodeposition.

The first full paragraph on page 81 (lines 11-15) is amended as follows:

It can be seen from the data in [Table 1] Figure 4 that, of the above-mentioned four different electroplating techniques, the constant-voltage pulse plating technique provides the highest electrodeposition uniformity.

The paragraph bridging pages 136 and 137 is amended as follows:

As to the multilayer printed circuit board according to Example 17, solder bumps 6076U, 6076D were disposed at the position a little far from the plated-through holes 6036. On the other hand, as to the multilayer printed circuit board according to Example 22, solder bumps 6O76U, 6076D were disposed immediately over the upper via holes 6160. Therefor, the multilayer printed circuit board according to Example [21] 22 had an advantage that the plated-through hole 6036, lower-layer via hole 6060, upper-layer via hole 6160and solder bumps 6076U, 6076D can be lined up in good registration so that the wiring length can be reduced to increase the transmission speed of signals, and a large amount of power can be obtained instantaneously from the power layer.

IN THE CLAIMS:

Claims 1-8, 14-21, 27-31, 34-36, 39 and 47 are canceled.

The claims are amended as follows:

9 (Amended). A circuit board comprising a substrate and[, as] built thereon, a circuit comprised of a copper film,

wherein said copper film comprises an electroplated layer and has properties that (a) its crystallinity is such that the X-ray diffraction half-width of the (331) plane of copper is less than 0.3 deg. and (b) the variation in thickness ((maximum thickness-minimum thickness)/average thickness) of said copper film as measured over the whole surface of said substrate is not greater than 0.4.

11 (Amended). A printed circuit board comprising a substrate and, [as] built thereon, a circuit comprised of a [plated] copper film,

wherein said [plated] copper film comprises an electroplated layer and has properties that (a) its crystallinity is such that the X-ray diffraction half-width of the (331) plane of copper is less than 0.3 deg. and (b) the variation in thickness ((maximum thickness-minimum thickness)/average thickness) of said copper film as measured over the whole surface of said substrate is not greater than 0.4.

12 (Amended). A printed circuit board comprising a substrate formed with a conductor circuit, an interlayer resin insulating layer [built] thereon and a conductor circuit comprised of a copper film [as built] on said interlayer resin insulating layer and having [vial] via holes by which said conductor circuits are interconnected,

wherein said copper film comprises an electroplated layer and has properties that (a) its crystallinity is such that the X-ray diffraction half-width of the (331) plane of copper is less than 0.3 deg. and (b) the variation in thickness ((maximum thickness-minimum thickness)/average thickness) of said copper film as measured over the whole surface of said substrate is not greater than 0.4.

13 (Amended). The printed circuit board according to Claim 11 [or 12] wherein said copper film has an elongation of not less than 7%.

22 (Amended). A printed circuit board comprising a resin insulating substrate board formed with a roughened surface and, [as built] thereon, a conductor circuit comprising at least an electroless plated film, wherein said electroless plated film has a stress of 0 to +10 kg/mm^2.

23 (Amended). A printed circuit board comprising a resin insulating substrate board formed with a roughened surface and, [as] built thereon by semi-additive process, a conductor circuit comprising at least an electroless plated film,

wherein said roughened surface comprises convex areas and concave areas, and said electroless plated film is complementary to said roughened surface with [the] said electroless plated film in convex areas of [the] said roughened surface being relatively greater in thickness than said electroless plated film in concave areas of said roughened surface.

24 (Amended). A printed circuit board comprising a substrate board formed with a lower-layer conductor circuit and, [as] built thereon, an upper-layer conductor circuit through the intermediary of an interlayer resin insulating layer, with said upper-layer conductor circuit and said lower-layer conductor circuit being interconnected by via holes,

wherein said upper-layer conductor circuit comprises at least an electroless plated film, said interlayer resin insulating layer is provided with a roughened surface, with said electroless plated film [is] being complementary to said roughened surface, and

said interlayer resin insulating layer and [bottoms of] said via holes are [also] provided with [an] the same electroless plated film, with said electroless plated film formed on the bottoms of said via holes having a thickness equal to 50 to 100% of the thickness of [the] said electroless plated film on said interlayer resin insulating layer.

25 (Amended). A printed circuit board comprising a resin insulating substrate board and[, as built] thereon[,] a conductor circuit comprising at least an electroless plated film,

wherein said electroless plated film [comprises] is a copper film, and comprises at least one metal species selected from the group consisting of nickel, iron and cobalt.

32 (Amended). A multilayer printed circuit board comprising a core board having a conductor circuit and, [as built] over said conductor circuit, [a] buildup wiring layers [obtainable by building up] comprising alternating an interlayer resin insulating layer and a conductor layer thereon, [alternately with] wherein the conductor layers [being] are interconnected by via holes,

wherein said core board comprises a copper-clad laminate, [the] said conductor circuit [on said core board] comprises [the] a copper foil of said copper-clad laminate and a plated metal layer, [and]

the thickness of [the] said conductor circuit [on said core board] is not greater by more than 10 μm than the thickness of [the] said conductor layer on said interlayer resin insulating layer, and

the thickness of said conductor circuit is substantially the same as the thickness of said conductor layer on said interlayer resin insulating layer.

37 (Amended). A multilayer printed circuit board comprising a core board and[, as constructed] on both sides thereof, buildup wiring layers [obtainable by building up] comprising alternating an interlayer resin insulating layer and a conductor layer thereon, [alternately with] wherein said conductor [layers] layers [being] are interconnected by via holes,

wherein said core board is provided with plated-through holes, said via holes are formed immediately over said plated-through holes in the manner of plugging

the through holes in said plated-through holes [in said core board] and are interconnected with said plated-through holes.

40 (Amended). A multilayer printed circuit board comprising a core board and[, as constructed] on both sides thereof, [a] buildup wiring layers [obtainable by building up] comprising alternating an interlayer resin insulating layer and a conductor layer thereon, [alternately with via holes interconnecting] wherein the conductor layers are interconnected by via holes,

[wherein the via holes in a lower layer are disposed immediately over the plated-through holes in said core board and via holes in an upper layer are disposed immediately over said via holes in the lower layer]

wherein said core board is provided with plated-through holes, and lower-layer via holes are disposed immediately over said plated-through holes, said plated-through holes being interconnected with said lower-layer via holes, and upper-layer via holes are disposed immediately over said lower-layer via holes, said upper-layer via holes being interconnected with said lower-layer via holes.

41 (Amended). A multilayer printed circuit board comprising a core board and, [as constructed] on both sides thereof, [a] buildup wiring layers [obtainable by building up] comprising alternating an interlayer resin insulating layer and a conductor layer thereon, [alternately with via holes interconnecting] wherein the conductor layers are interconnected by via holes,

wherein said core board is provided with plated-through holes, and said plated-through holes [of core board] are filled with a filler, with the [surfaces] surfaces of said filler which are exposed from said plated-through holes being covered with [a] said conductor layer provided with lower-layer via holes, and upper-layer via holes [being] are disposed immediately over said lower-layer via holes, said lower-layer via holes being interconnected with said upper-layer via holes.

42 (Amended). A multilayer printed circuit board comprising a core board and, [as constructed] on both sides thereof, [a] buildup wiring layers [obtainable by building up] comprising alternating an interlayer resin insulating layer and a conductor layer thereon, [alternately with via holes interconnecting] wherein the conductor layers are interconnected by via holes,

[wherein via holes in a lower layer are disposed to plug the through holes of plated-through holes in said core board, with via holes in an upper layer being disposed immediately over said via holes in the lower layer]

wherein said core board is provided with plated-through holes, and lower-layer via holes are disposed to plug through holes of said plated-through holes, said plated-through holes being interconnected with said lower-layer via holes, and upper-layer via holes are disposed immediately over said lower-layer via holes, said upper-layer via holes being interconnected with said lower-layer via holes.

44 (Amended). The multilayer printed circuit board according to any of Claims 40 to 43, wherein said lower-layer via holes are filled with metal.

Claims 48-57 are added as new claims.